A 56GS/s 8-bit Time-Interleaved Analog to Digital Converter

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***Abstract*—This paper presents a 56GS/s 8-bit time-interleaved analog to digital converter (ADC) with an integrated JESD204B interface implemented in the 28nm RF CMOS node. ADC block architectures, advanced calibration techniques, a top-level layout, a chip carrier, and initial considerations for the test printed circuit board (PCB) are discussed. Based on the simulation results, the ADC core achieves the expected 6-bit value of effective number of bits (ENOB) at 56GS/s at an input frequency of 20GHz while dissipating 420mW. On-chip calibration mechanisms are employed in the ADC to suppress the spurs in the ADC output spectrum caused by the usage of time-interleaving techniques. This feature extends the ADC's application to phased array radars, radio telescopes, and 100Gb/s fiber optic receivers.**

Keywords—successive approximation analog to digital converter; high sampling rate ADC; time-interleaved ADC; JESD204B.

I. INTRODUCTION

Low-power moderate resolution high sampling rate analog to digital converters (ADCs) are in high demand for wireless and wireline communication systems. Time-interleaved ADC architectures have been employed to boost the overall ADC performance while relaxing the sampling rate required for each sub-ADC. However, time interleaving activity results in spurious response in the combined multi-ADC output spectrum, if the sub-ADC gains, sampling clock timing, and successive approximation register (SAR) comparator offsets are not perfectly matched. Minimizing these effects with circuits of limited performance presents unique challenges that have led to innovative solutions in the ADC implementation.

II. ADC ARCHITECTURE

A. Interleaving Factors and Sampling Clocks

An incoming analog signal to the ADC is supplied to a differential 4x interleaved sampler running on both phases of a 14GHz clock (see the block diagram in Fig. 1). The sampling clock is formed by dividing the internally generated 28GHz clock frequency by 2. The 28GHz clock is generated by an internal phase-locked loop (PLL) multiplying the low jitter 1GHz or 2GHz reference clock by a factor of 28 or 14, respectively. We chose to have 64 interleaved SAR ADCs, each running at 875MHz as a compromise between die size, power dissipation, and sub-ADC performance when implemented at the 28nm CMOS node. The 8-bit data from each sub-ADC is organized into frames in compliance with the JESD204B standard and is supplied to 64 current mode logic (CML) output buffers each running at 8.75Gb/s. The required 4.375GHz clock is derived by multiplying the 500MHz clock by 35 and dividing the resulting 17.5GHz clock frequency by 4. The required 500MHz reference clock for this PLL is obtained by dividing the 1GHz or 2GHz reference clock by 2 or 4, respectively. To minimize power dissipation, a pseudo differential CMOS signaling is applied for clock distribution.

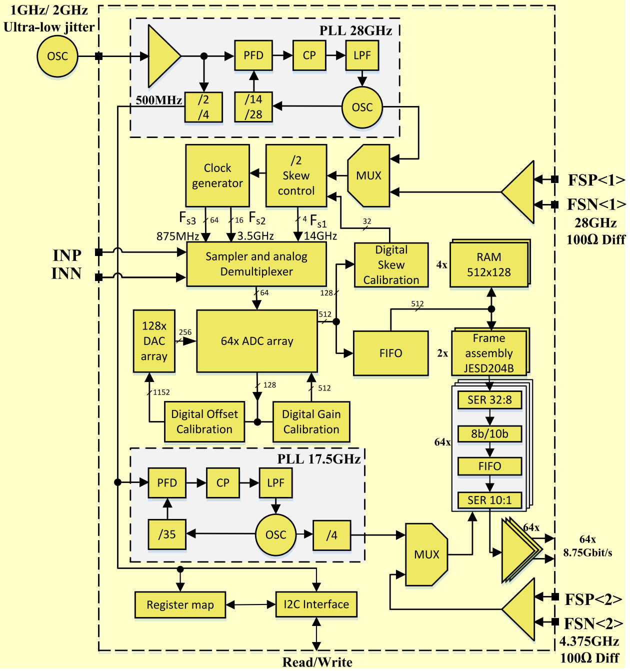
1GHz/ 2GHz
Ultra-low jitter
OSC
PLL 28GHz
PFD
CP
LPF
500MHz
/2
/4
/14
/28
OSC
Clock generator
/2 Skew control
MUX
FSP<1>
FSN<1>
28GHz
100Ω Diff
Fs3
64
16
Fs2
4
Fs1
875MHz
3.5GHz
14GHz
32
INP
INN
Sampler and analog Demultiplexer
Digital Skew Calibration
4x
RAM 512x128
64
128
512
128x DAC array
256
64x ADC array
512
FIFO
2x
Frame assembly JESD204B
1152
128
512
Digital Offset Calibration
Digital Gain Calibration
SER 32:8
8b/10b
FIFO
SER 10:1
64x
PLL 17.5GHz
PFD
CP
LPF
/35
OSC
/4
MUX
64x
64x
8.75Gbit/s
Register map
I2C Interface
FSP<2>
FSN<2>
4.375GHz
100Ω Diff
Read/Write

Fig. 1. A block diagram of the 56GS/s 8-bit time-interleaved SAR ADC.

B. Time Interleaving Related Spur Suppression

Suppressing the spurs in the ADC's output spectrum requires to apply advanced mixed signal calibration techniques. We implemented on-chip calibration mechanisms for the three major contributors to the spurious response: sub-ADC gain mismatch, sampling clock phase skew error, and comparator offset. The method we use to detect gain error signals involves correlating the digital output data of each sub-ADC versus a master sub-ADC. This data are later integrated over many conversion cycles of the ADC. The gain mismatch is corrected by adjusting the reference voltage to each sub-ADC. Another version of the same basic method is used to detect the sampling clock skew error. The error is corrected by adjusting the sampling clock skew for the 4 phase interpolators. A unique aspect in our ADC calibration scheme is that it does not require precise analog training signals to be applied to the ADC input.

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Therefore, the ADC can use the application related input signals to perform calibrations as needed. Since circuit component parameters can drift over time, we find this recalibration feature particularly appealing especially in harsh operating environments such as space.

The time interleaving related spurs resulting from the comparator offset are corrected inside each sub-ADC through a special DC biased diff pair connected in parallel with the comparator's main diff pair. A voltage digital to analog converter (DAC) slowly offsets the correction diff pair over many conversion cycles until a zero crossing is consistently detected at the output of each comparator. This indicates that the offset has been minimized to within the range of 1-LSB of the DAC output voltage. The comparator offset correction is performed in the spare time between the SAR conversion cycles of each sub-ADC. By setting the appropriate register bits, all three calibration loops we discussed can either be set to run in the background or remain frozen after the initial start-up calibration.

C. Sub-ADC Design

Sub-ADCs employ dual interleaved Strong-Arm based comparators clocked on the edges of clock signals clk_cmp1 and clk_cmp2 as shown in Fig. 2. While one comparator is working, the other is in the reset mode to improve performance. The transistors in the comparator and latch were sized seeking to meet metastability time constant requirements when small signals are applied to the inputs for the lower bits (LSB). The programmable reference voltage generator (Fig. 2) is used to adjust the ADC gain during the calibration mode. Due to limitations in the available standard digital cell library, the SAR logic block was custom designed based on pre-charged logic cells which were further optimized using an analog simulator. These modifications allow the sub-ADC to be run at 875MHz with a sufficient frequency margin.

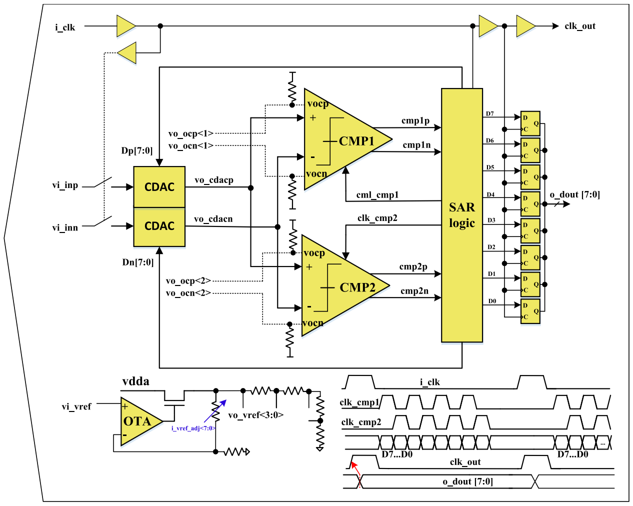

Fig. 2. A simplified block diagram of a sub-ADC.

D. Calibration Impact on ADC Performance Simulation

The array of 64 time-interleaved sub-ADCs when implemented on a chip are subject to process gradients and device parameter mismatch. In order to avoid occurrence of interleaving related spurs in the ADC's output spectrum due to these variations, the sub-ADCs must be calibrated. The ADC output spectrum simulated before (red curve) and after (blue curve) comparator offset calibration can be seen in Fig. 3. Based on the post calibration results, the spurs are reduced by approximately 30dB.

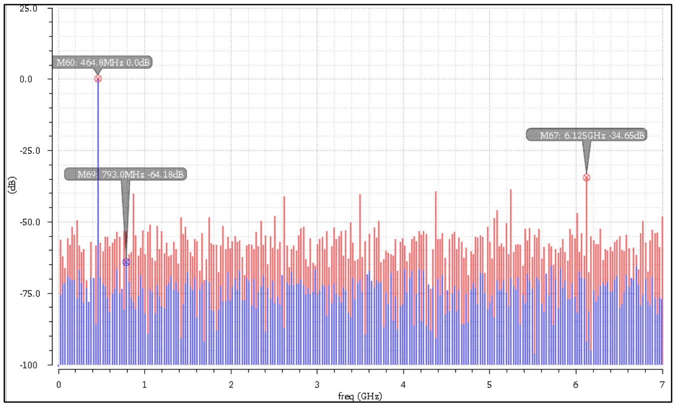

Fig. 3. The ADC output spectrum before (red) and after (blue) calibration.

To observe the effective number of bits (ENOB) value dependence on the comparator offset mismatch in an interleaved ADC, we swept the offset correction DAC's output voltage from its minimum to maximum value. The results of this experiment are presented in Fig. 4. The red curve shows the ENOB value before calibration, and the blue curve shows the results after calibration. As can be seen, comparator offset increasing beyond +/-1mV begins to reduce the ENOB value below our targeted 6-bit for the entire ADC. After calibration, the ENOB value remains at approximately 7.8-bit over the entire +/-2mV offset range, which was determined through Monte-Carlo simulations as the maximum value we might encounter at +/-3σ extremes of process parameters. Therefore, calibration is of crucial importance in maximizing the ADC performance.

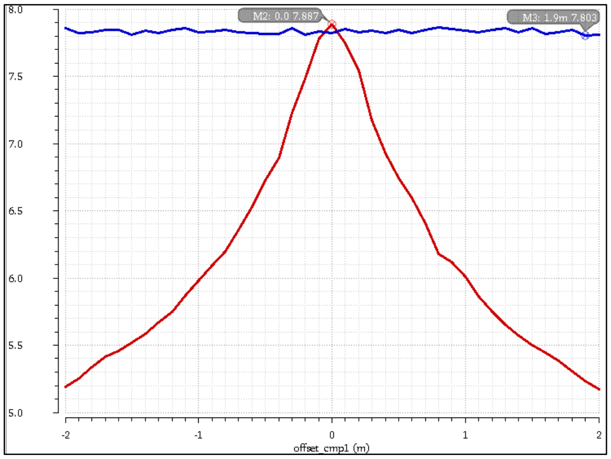

Fig. 4. ADC ENOB value vs. comparator offset (red). Calibration enabled (blue).

A similar simulation was performed to quantify the effects of sub-ADC gain error. The simulated output spectrum of the ADC can be seen in Fig 5. The blue trace represents the spectrum before the ADC calibration and the red trace indicates results after calibration. As can be seen, the spur is suppressed by approximately 28dB.

In our gain calibration scheme, all sub-ADCs are matched to a master sub-ADC. To visualize the ENOB sensitivity to the gain mismatch, the ENOB value was simulated and plotted versus the gain correction DAC adjustment range (Fig. 6). The local maximum on the ENOB value is the target for the digital calibration loop. If necessary, this value can be overwritten by changing the I2C register values. To reduce the simulation time, these tests were performed on an array of 16 rather than 64 sub-ADCs.

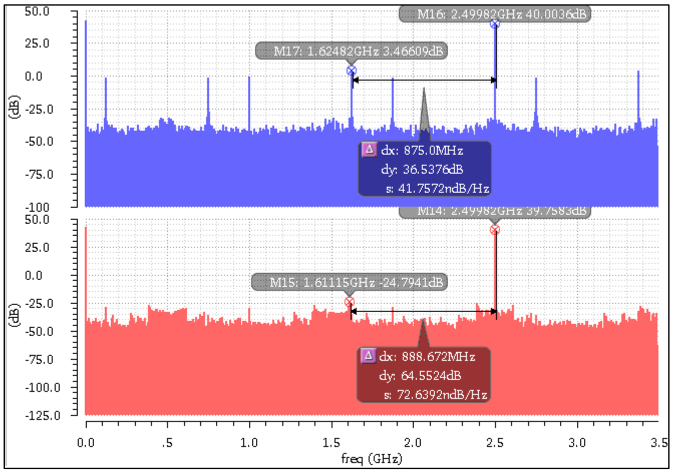

Fig 5. The ADC output spectrum before (blue) and after (red) gain calibration.

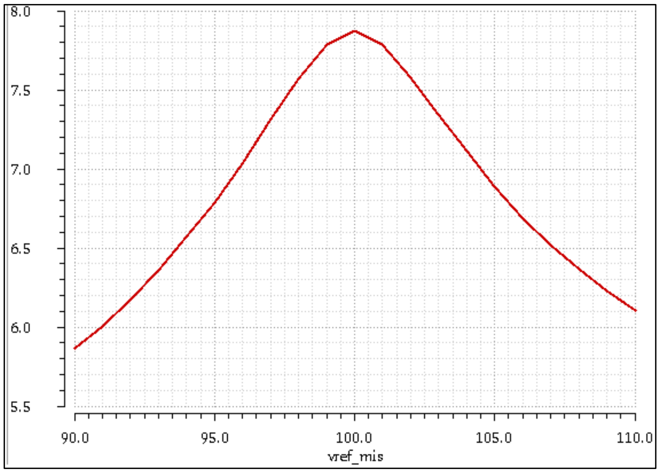

Fig. 6. ADC ENOB value vs. sub-ADC's gain offset, which is a function of the VREF.

At a system level, once the sub-ADC gain and comparator offsets are calibrated, we must then calibrate any timing phase errors in the sampling clocks to avoid formation of additional time-interleaving related spurs. The clocking distribution scheme can be seen in Fig. 7. The analog input samplers are clocked by the four phases derived from a 28GHz clock (bottom left). Phase interpolators are used to adjust the position of each clock's falling edge until they match. The phase interpolators are based on a differential topology, however, their outputs are converted from differential to single ended to drive the input signal samplers. Circuit topology and device sizes in the differential to single ended converter are also optimized for low noise operation. To implement the conversion of the differential signal to full-swing single-ended signal, we used an AC coupled inverter with a resistive feedback, since this circuit offers both low noise operation and low power consumption.

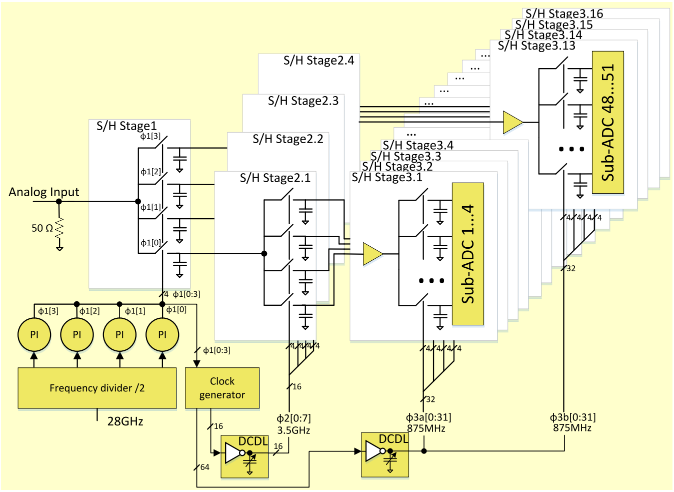

Fig. 7. ADC top level clock distribution scheme.

Both random and deterministic jitter are critical parameters in the first stage sampler. However, the subsequent stages are much less sensitive to the jitter since the signal has already been sampled in the first stage. The following stages are simply passing the pseudo DC analog voltages to the 64 sub-ADCs. Since the clock for the first sampler passes through phase interpolators, their noise contribution must be included in our total jitter estimations. The PLL and phase interpolators have been designed for low noise operation seeking to improve the thermal and 1/f induced jitter. Since full swing CMOS circuits are involved, the deterministic jitter caused by power supply noise will also have a significant effect.

To suppress the noise coupled on the power supply buses, we applied bypass capacitors to the power supply nodes within the chip, the chip carrier in the direct proximity to the chip and on the printed circuit board (PCB). The decoupling capacitance inside the chip, although substantial in value, has a lower quality factor since the low voltage MOS gates used as capacitors need to be protected from overvoltage conditions during electrostatic discharge (ESD) events. These gates are protected by pass gate devices that disconnect each MOS-cap gate from the power supply bus when the chip is powered down.

Another measure taken inside the chip to reduce noise coupling was the separation of power supply buses for critical blocks. For further noise isolation, the PLL, phase-frequency detector (PFD), and digital blocks are located in separate deep n-wells, while the ADC core is implemented in the main substrate. At the board level, the power supply for this chip is expected to be supplied by a linear regulator, while most systems are powered by switching type regulators for efficiency. When the chip is integrated into a larger system, care needs to be taken to prevent tones from coupling into the ADC's power supply.

III. PHYSICAL IMPLEMENTATION

The chip is fabricated in the 28nm high performance computing (HPC) CMOS node from TSMC (Fig. 8). The chip physical area is 2.8mm x 2.8mm.

Analog differential signal is supplied to the ADC inputs through the solder bumps located on the chip's top, just above the ADC block. The coils located next to the solder bumps are used for cancelling out input capacitance of the sampler, thus improving S11. A bias block is located on the left side of the ADC. The PLL for synthesizing the ADC clock is placed on the right side. The PLL block's function is to generate a 28GHz clock which is divided-by-2 to form the four sampling clock phases used in the Stage 1's interleaved sampler. An external clock multiplexer (MUX) is also provided for bypassing the PLL in case it fails or to run the ADC at a lower frequency during testing if needed. The visible set of 3 inductors (top right on the chip's layout) are used for the 28GHz voltage-controlled oscillator (VCO) LC tank and jitter filter. To the left of the VCO, we have placed a 28GHz output buffer which employs two more inductors. The buffer passes the 28GHz clock through a transmission line to the frequency divider by-2 located at the ADC's sampling clock input. This is one of the most critical parts in the entire chip, since the clock jitter must be minimized, and the amplitude must remain large enough to drive the divider by-2 at any PVT corner and wide statistical spread of component parameters.

Digital calibration blocks and state machines, including the random-access memory (RAM) blocks are implemented below the ADC block. The 8-bit output data words from each SAR sub-ADC are sent into the transmitters to be serialized and distributed to the JESD204B compliant interface blocks (marked by red). Due to the sophisticated data serializing and formatting to comply with the JESD20B specifications, these blocks occupy approximately 75% of the total chip area. The serializer PLL required for synthesizing clock for the JESD204B interface is located on the lower side of the chip. Above this PLL, we located the I2C controller. Space between blocks is filled with digital glue logic and power supply decoupling capacitors.

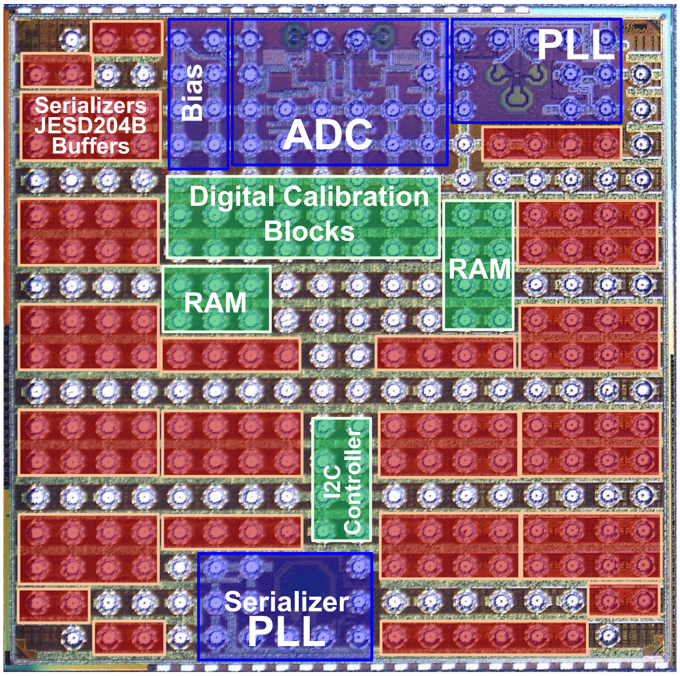

Fig. 8. A photo of the 56GS/s 8-bit interleaved SAR ADC chip.

IV. CHIP CARRIER AND EVALUATION SETUP

A. *High-Speed Chip Carrier*

The chip carrier is required to pass a 28GHz analog input signal to the ADC through a delay matched differential transmission line while signal power losses in the dielectric should be minimized. A total of 64 x 8.75Gbps differential data lines must also be accommodated on the same substrate. These requirements call for a special chip carrier for the ADC. The chip carrier was developed based on a low Dk, low dielectric loss low temperature co-fired ceramic (LTCC) process with low metal sheet resistance conductors. This permits reducing the metal trace width and distance between traces used for 50Ω (100Ω differential) impedance transmission lines which made possible shrinking the substrate size to approximately 12.8mm x 12.8mm while using 17 layers (Fig. 9). The chip carrier also holds 33 capacitors for power supply bypass. The capacitors are selected to have their self-resonant frequency (SRF) value matching the frequencies of the signals which may be coupled to the power supply buses. The S11 and S21 parameters for the transmission lines leading to the ADC input were simulated up to 28GHz and confirmed to be below -18dB and above -1dB, respectively. The length of the impedance-controlled wires used to pass the 8.75Gbps ADC output data was matched to within 0.2mm accuracy for the direct and inverted signals. The S11 and S21 parameters for these interconnects are respectively below -13dB and above -0.7dB up to 7GHz. Besides high electrical performance, the selected LTCC process features a high temperature expansion coefficient which closely matches that of the PCB, thus ensuring better reliability of the assembly.

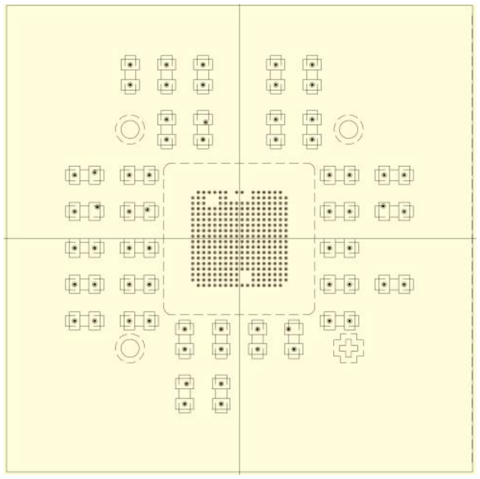

Fig. 9. A chip carrier design drawing - top view.

B. *Evaluation Setup*

The characterization of the 56GSps ADC requires a special board (Fig. 10). The board holds a custom high-bandwidth socket for housing the device under test (DUT), power regulators, a reference voltage source, a programmable system on chip (PSoC) for ADC control/diagnostics and structures for transmission line parameter evaluation. The board also includes the reference clock input, a sampling clock input to be used for bypassing the internal PLL and optional frequency dividers to be used to bypass the JESD204B PLL. The board is made of Megtron-6 material seeking to minimize signal losses. To

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minimize discontinuities along the high-speed input signal path, the length of the interconnects is minimized. A dual edge-launch sub-miniature push-on micro (SMPM) connector is used to ensure matching of the interconnect length for the direct and inverted ADC inputs. A pair of 6-inch length matched cables will be used to feed the signal to the ADC input. ADC data outputs are routed to 64 pairs of sub-miniature version A (SMA) connectors with surface soldered signal interconnects which are used to handle 8.75Gbps data rate per channel. The connectors are located on three sides of the board. This connector placement is optimized for the ADC evaluation board to conveniently mate with a field programmable gate array (FPGA) development board which is required to acquire and process the 64 x 8.75Gbps data from the ADC.

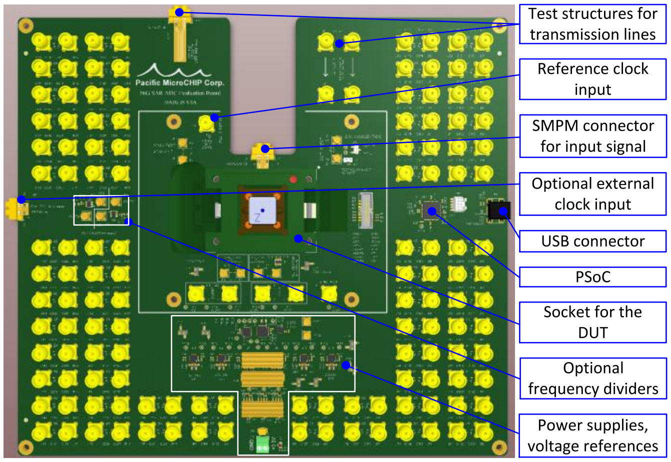
Test structures for transmission lines
Reference clock input
SMPM connector for input signal
Optional external clock input
USB connector
PSoC
Socket for the DUT
Optional frequency dividers
Power supplies, voltage references
Pacific MicroCHIP Corp.

Fig. 10. Design of the test board for the 56GS/s ADC evaluation.

C. Expected Performance

Compared to the state-of-the-art devices (Table 1), our ADC features much wider input signal bandwidth (30.1GHz vs. 19.9 GHz [2]) and higher ENOB value while consuming less power (420mW vs. 667mW [2]). Another advantage of our ADC is that it integrates the industry standard JESD204B interface for convenient data transfer to FPGAs and ASICs. Our device also allows the users to utilize any incoming signal as stimulus for calibrating the internal blocks, thus permitting to simplify system integration.

TABLE I. HIGH SPEED ADC ASIC SUMMARY.

	Time-interleaved ADC		
	This device	***ISSCC 2017[1]***	***ISSCC 2014[2]***
Architecture	TI-SAR	TI-SAR	TI-SAR
Power supply	0.9V	-	1.2V
Sampling rate	56GS/s	64GS/s	90GS/s
Resolution	8-bit	8-bit	8-bit
Power consumption	420mW	950mW	667mW
Input bandwidth (-3dB)	30.1	19	19.9
ENOB @ 20GHz	6.1	5.3	SNDR 33dB
On-chip area	1.05mm^2	2mm^2	0.45mm^2
Calibrations	Gain Offset Time-Skew	Gain Offset Time-Skew	Gain Offset Time-Skew

D. Application Block Diagram

The ADC application block diagram is presented in Fig. 11. The evaluation board includes low-dropout (LDO) regulators for the ADC powering, an analog voltage measurement circuit for chip test outputs, the Xilinx FPGA evaluation board for data acquisition, processing and for chip control, a source of low jitter reference clock (Rakon LNO1000 or LNO2000). The clock source by Rakon is a high-performance low jitter SAW oscillator used as a reference clock for an integrated 28GHz PLL. The I2C interfacing and scan chain test mode are implemented through the FPGA. The test output measurement block is based on Cypress PSOC CY8C58LP. It is used to measure voltage from on-chip analog test points, from on-chip and off-chip analog temperature sensors, and to apply external reference voltage to the on-chip test points.

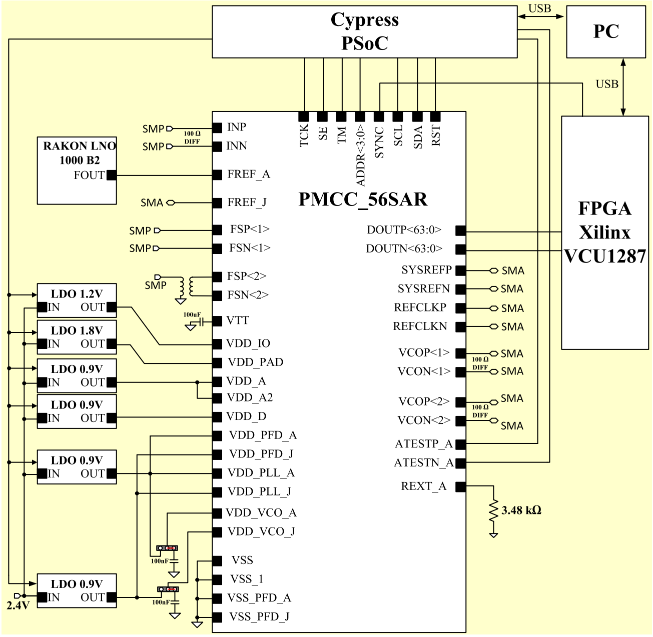
Cypress PSoC
PC
USB
USB
FPGA Xilinx VCU1287
PMCC_56SAR
RAKON LNO 1000 B2
FOUT
SMP
SMP
100 Ω DIFF
SMA
SMP
SMP
SMP
100nF
INP
INN
FREF_A
FREF_J
FSP<1>
FSN<1>
FSP<2>
FSN<2>
VTT
VDD_IO
VDD_PAD
VDD_A
VDD_A2
VDD_D
VDD_PFD_A
VDD_PFD_J
VDD_PLL_A
VDD_PLL_J
VDD_VCO_A
VDD_VCO_J
VSS
VSS_1
VSS_PFD_A
VSS_PFD_J
TCK
SE
TM
ADDR<3:0>
SYNC
SCL
SDA
RST
DOUTP<63:0>
DOUTN<63:0>
SYSREFP
SYSREFN
REFCLKP
REFCLKN
VCOP<1>
VCON<1>
VCOP<2>
VCON<2>
ATESTP_A
ATESTN_A
REXT_A
3.48 kΩ
SMA
100 Ω DIFF
LDO 1.2V
LDO 1.8V
LDO 0.9V
LDO 0.9V
LDO 0.9V
LDO 0.9V
IN
OUT
100nF
2.4V

Fig. 11. ADC application block diagram.

ACKNOWLEDGMENT

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REFERENCES

[1] Jun Cao et al., “A Transmitter and Receiver for 100Gb/s Coherent Networks with Integrated 4×64GS/s 8b ADCs and DACs in 20nm CMOS,” ISSCC, pp. 484-485, February 2017.

[2] Lukas Kull et al., “A 90GS/s 8b 667mW 64× Interleaved SAR ADC in 32nm Digital SOI CMOS,” in ISSCC, pp. 378-379, February 2014.